WHAT IS CLAIMED IS:

1. A memory device comprising:

a plurality of normal memory cells;

a plurality of spare memory cells used instead of a defective memory cell when said defective memory exists in said plurality of normal memory cells;

a plurality of bit lines used for reading data from said plurality of normal memory cells;

a read amplifying circuit reading data from said plurality of normal memory cells and said plurality of spare memory cells;

a plurality of data lines for connecting said plurality of bit lines to said read amplifying circuit; and

a connecting circuit forming parts of paths connecting said plurality of data lines to said plurality of normal memory cells and said plurality of spare memory cells so as to substantially equalize load capacitance of said plurality of data lines, wherein

said connecting circuit not only connects a first selected bit line among said plurality of bit lines to be selected according to a first input address to a first data line among said plurality of data lines, but also forms parts of paths that connect a part of said plurality of spare memory cells to be selected according to said first input address to a second data line different from said first data line among said plurality of data lines, and also not only connects a second selected bit line among said plurality of bit lines to be selected according to a second input address to said second data line, but also forms parts of paths that connect a part of said plurality of spare memory cells to be selected according to said second input address to said first data line.

2. The memory device according to claim 1, further comprising:

first and second spare bit lines for reading data from said plurality of spare memory cells, wherein

said connecting circuit includes:

a first column select gate connecting said first selected bit line to said first data line according to said first input address;

a second column select gate connecting said second spare bit line to said second data line according to said first input address;

a third column select gate connecting said second selected bit line to said second data line according to said second input address; and

a fourth column select gate connecting said first spare bit line to said first data line according to said second input address.

3. The memory device according to claim 1, further comprising:

a spare bit line for reading from said plurality of spare memory cells, wherein

said connecting circuit includes:

a first column select gate connecting said first selected bit line to said first data line according to said first input address;

a second column select gate connecting said spare bit line to said second data line according to said first input address;

a third column select gate connecting said second selected bit line to said second data line according to said second input address; and

a fourth column select gate connecting said spare bit line to said first data line according to said second input address.

4. The memory device according to claim 1, further comprising:

a decode circuit not only selecting first and second access memory cells among said plurality of normal memory cells connected to said first and second selected bit lines, respectively, according to an address signal, but also performing selection of portions corresponding to said first and second access memory cells from said plurality of spare memory cells.

5. The memory device according to claim 1, wherein

each of said plurality of normal memory cells and said plurality of spare memory cells changes an electric resistance value according to write data, and

said read amplifying circuit detects a change in said electric resistance value.

6. The memory device according to claim 1, wherein

each of said plurality of normal memory cells and said plurality of spare memory cells includes a magnetic storage element.

7. A memory device comprising:

a plurality of memory cells storing information by a change in respective electric resistance, and arranged in one memory cell array;

a read amplifying circuit performing parallel data reading from a plurality of selected memory cells selected simultaneously among said plurality of memory cells; and

a current path forming section forming a plurality of read current paths respectively corresponding to said plurality of selected memory cells between said read amplifying circuit and a supply source of a power supply potential, wherein

said plurality of read current paths are separated from each other at least in said memory cell array.

8. The memory device according to claim 7, wherein

a part of said plurality of memory cells are spare memory cells each used instead of a defective memory cell when said defective memory exists in normal memory cells among said plurality of memory cells, and

said plurality of selected memory cells includes:

said normal memory cells; and

said spare memory cells.

9. The memory device according to claim 7, wherein

said current path forming section includes: a plurality of source lines giving reference potentials for data reading to each of said plurality of selected memory cells, and

said plurality of source lines are separated from each other at least

in said memory cell array.

10. The memory device according to claim 9, wherein

first and second selected memory cells among said plurality of selected memory cells are both placed on a first row in said memory cell array,

first and second source lines, among said plurality of source lines, provided correspondingly to said first and second selected memory cells, respectively, are geometrically interchanged therebetween so that in a first region where said first memory cell is arranged, said first source line is placed along said first row and said second source line is placed along a second row adjacent to said first row, while in a second region where said second memory cell is arranged, said second source line is placed along said first row and said first source line is placed along said second row.

11. The memory device according to claim 9, wherein

first and second selected memory cells among said plurality of selected memory cells are placed on first and second rows, respectively, in said memory cell array,

first and second source lines, among said plurality of source lines, provided correspondingly to said first and second selected memory cells are placed along said first and second rows, respectively, and

said memory device further comprising:

a first select line for selecting both of said first and second selected memory cells; and

a second select line provided adjacent to said first select line, wherein

said first select line and said second select line are geometrically interchanged therebetween at some midpoint on said first select line so that said first select line is placed along said first row in a first region where said first selected memory cell is arranged, while being placed along said second row in a second region where said second selected memory cell is arranged.

12. The memory device according to claim 9, wherein

first and second selected memory cells among said plurality of selected memory cells are placed both on a first row in said memory cell array, and

first and second source lines among said plurality of source lines, provided correspondingly to said first and second selected memory cells, respectively, are both placed obliquely to said first row in parallel to each other.

13. The memory device according to claim 9, wherein

first and second selected memory cells among said plurality of selected memory cells are placed on first and second rows, respectively, in said memory cell array,

first and second source lines among said plurality of source lines, provided correspondingly to said first and second selected memory cells, respectively, are placed along said first and second rows, respectively, and

said memory device further comprising: a first select line for selecting both of said first and second selected memory cells, wherein said first select line is placed obliquely to said first and second rows.

14. A memory device comprising:

a plurality of normal memory cells including respective electrically conductive magnetic elements;

a plurality of normal bit lines provided correspondingly to the plurality of columns each of normal memory cells;

a plurality of first reference memory cells connected to said the plurality of normal bit lines with one-to-one correspondence;

a plurality of spare memory cells each used instead of a defective memory cell when said defective memory cell exists in said plurality of normal memory cells;

a plurality of spare bit lines provided correspondingly to the plurality of columns of said spare memory cells;

a plurality of second reference memory cell connected to said

plurality of spare bit lines with one-to-one correspondence; and

a read circuit connected to four bit lines including a first bit line to which a memory cell to be read is connected, a second bit line selected from said plurality of normal bit lines other than said first bit line, a third bit line to which a spare memory cell corresponding to said memory cell to be read is connected and a fourth bit line selected from said plurality of spare bit lines other than said third bit line according to said address signal to generate a reference value for data reading through synthesis from first and second reference memory cells connected to the second and fourth bit lines, respectively.

15. The memory device according to claim 14, wherein

each of said plurality of normal memory cells takes first and second resistance values different from each other according to storage data,

each of said plurality of first reference memory cells takes said first resistance value, and

each of said plurality of second reference memory cells takes said second resistance value.

16. The memory device according to claim 15, wherein

each of said plurality of normal memory cells takes said first resistance value in an initial state thereof.

17. The memory device according to claim 15, wherein

each of said normal memory cell takes said first resistance value in an initial state thereof, and

each of said plurality of second reference memory cells includes:

an electrically conductive magnetic element taking said first resistance value; and

a fixed resistance taking a resistance value obtained by subtracting said first resistance value from said second resistance value.